

Clocktree RLC Extraction with Efficient Inductance Modeling

Norman Chang, Shen Lin, Lei He*, O. Sam Nakagawa, and Weize Xie

Hewlett-Packard Laboratories, Palo Alto, CA, USA

*University of Wisconsin, Madison, USA

Abstract. In this paper, we present an efficient yet accurate inductance extraction methodology and its application to clocktree RLC extraction. We first show that without loss of accuracy, the extraction problem of n traces with or without ground planes can be reduced to a number of one-trace and two-trace subproblems. We then solve one-trace and two-trace subproblems via a table-based approach. In particular, this method combined with linear cascading assumption have been applied successfully to the clocktree RLC extraction and optimization.

I. Introduction

Due to faster clock frequencies, shorter rise times, and lower resistivity metal (i.e. Cu), inductance effects of on-chip interconnects can no longer be ignored [1-2]. In particular, the inductance extraction is much needed for the clocktree modeling and simulation for high-frequency CPU designs [3]. This is due to the common design techniques of using much wider wires (can be sometimes more than 10 μ m in width) in clocktree routing to carry strong and fast-switching clock signals. The inductance effect in clocktree is worsen by the fact that large driver and therefore smaller source impedance is used to drive the clocktree. Therefore, the inductance (L) combined with RC extraction in clocktree is absolutely needed for better accuracy in clock skew simulation for high-frequency CPUs and ASICs. To illustrate the importance of including inductance in the clocktree simulation, we simulate a simple yet realistic configuration in Figure 1 without and with the inductance. The delays from the output of the clock buffer to the sink node are 28.01ps and 47.6ps respectively without and with the inclusion of inductance. The waveforms are displayed in Figure 2 and Figure 3. We can see that inductance is indeed needed in the simulation of a

clocktree to have a better estimation of the clock skew.

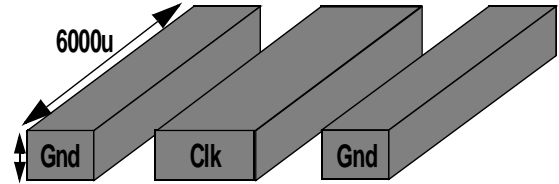


Figure 1: A co-planar waveguide clock net structure with wires of 6000 μ m long, 2 μ m thick, 10 μ m wide for the clock signal, and 5 μ m wide for the Gnd wires. The spacing between adjacent wires is 1 μ m. The clock buffer driving strength has about 40ohm as source resistance. An orthogonal signal layer is assumed to be below.

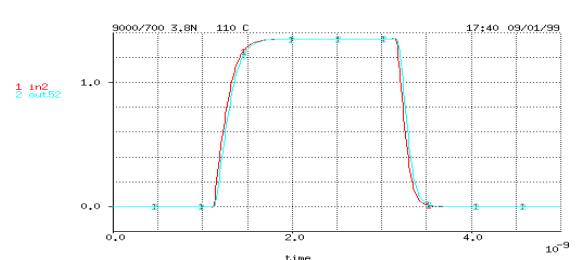


Figure 2: Waveforms at the output of the clock buffer and sink without inductance, i.e. RC netlist only.

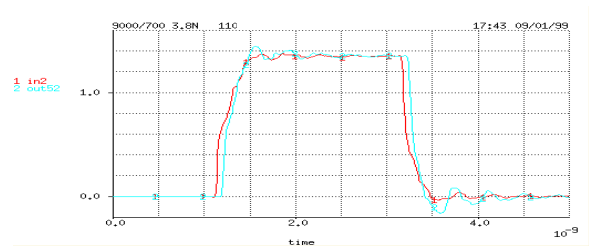


Figure 3: Waveforms at the output of the clock buffer and sink with inductance. The impact of overshoot and undershoot phenomenon on delay due to inductance can be observed.

A table based approach for on-chip inductance extraction combined with a fast generation of statistically-based RC models have been described in [4-5]. In this paper, we extend the approach described in [5] to model efficiently microstrip and stripline configurations often encountered in a clocktree design. We also solve the clocktree RLC extraction using the experimentally proven RLC-segment-based linearly cascaded method. In Section II, we review and extend the two basic foundations described in [5] which allow us to reduce the problem size of inductance extraction without loss of accuracy. In Section III, we propose a table-based inductance extraction methodology based on the two extended foundations. Linearly cascaded method is described in Section IV. In Section V, we present the application of this efficient inductance modeling method to clocktree RLC extraction. Section VI concludes this paper.

II. Foundations for Inductance Extraction

A. Two L_p (Partial Inductance) Extraction Foundations

There are multiple metal layers in a VLSI technology. We assume that wire traces in adjacent layers are orthogonal, and extract the inductance for a *block*, which contains n traces (T_1, T_2, \dots, T_n) of same lengths in the same layer N (see Figure 4). In addition, we also assume that the two most outside traces, T_1 and T_n , are dedicated AC grounded traces. When the block size is three, it is a coplanar-waveguide, which is one of the three basic forms for transmission line, and is often used for clock tree in high-speed designs. When the block size is large, it models the bus structure with outside ground traces that can be used for shielding only or for shielding and power supply at the same time. Because traces are orthogonal in adjacent layers, traces in layer $N+1$ and layer $N-1$ will not affect the inductance of traces in the current layer N [7]. However, there may be parallel traces or ground planes in layer $N+2$ and/or layer $N-2$ which can affect the inductance in layer N . We consider wide ground traces which can be treated as a local ground plane in layer $N+2$ and/or $N-2$.

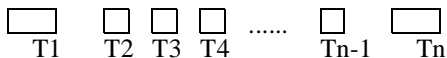


Figure 4: The cross-section view for a block of n traces, where T_1 and T_n are dedicated AC grounded traces. The width for each trace is W_1, W_2, \dots, W_n , and spacings are S_1, S_2, \dots, S_n .

Note that the capacitive effect is a “short-range” effect in the sense that for a block, only the mutual

capacitance between adjacent traces are important, and the rest of the mutual capacitance can be ignored. Therefore, for any trace, it is sufficient to solve the trace and its two adjacent traces via numerical extraction [6]. In other words, we are able to reduce the n -trace capacitance problem to a number of 3-trace subproblems. The inductive effect, however, is a “long-range” effect. As shown and proven in [5], when we do not specify which traces are ground traces, we compute partial inductance (denoted as L_p) under the PEEC model [7-9] and let the SPICE determines return path at simulation. In general, we have the following foundations for on-chip interconnects:

Foundation 1 Self L_p of a trace is *solely* decided by the trace (its length, width and thickness).

Foundation 2 Mutual L_p of two traces is *solely* decided by the two traces (their lengths, widths and thicknesses, and the spacing between them).

The above two foundations have been proven in [5] without consideration of the ground plane(s) in layer $N+2$ and/or $N-2$. When there are local ground planes below and/or above the *block* in layer N , we have the following extensions of Foundations.

B. Extension of Foundations

Foundation 1 and **Foundation 2** are still valid if we explicitly model the power/ground (either continuous or densely mesh) planes using the PEEC model. It leads to a model with a high complexity however. The key is that approximately, foundations similar to **Foundation 1** and **Foundation 2** hold for the loop inductance considering only the ground plane(s) as the merged ground nodes with the far end sink nodes of the traces (signal as well as shielding AC grounded traces in layer N) in the PEEC model. Therefore, we are still able to build the self inductance table with two dimensions (width and length), and the mutual inductance table with four dimensions (two widths, spacing and length), but the loop inductance rather than the partial inductance is pre-computed and stored for each structure of the microstrip or strip line. Because the loop inductance has taken the effect of power/ground planes into account, there is no need to explicitly model the inductance for power/ground planes for the final RLC model. Figure 5 shows a simulation example to illustrate the extension of the **Foundation**.

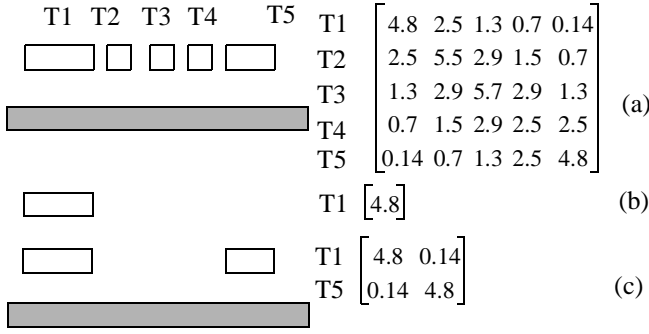


Figure 5: Loop inductance ($\times 0.1\text{nH}$) for (a) an array in layer N with a ground plane in layer $N-2$, (b) trace $T1$ only, and (c) two traces $T1$ and $T5$. From (b), one can observe that Foundation 1 is valid. From (c), we prove that Foundation 2 holds in simulation.

III. Table-based Inductance Extraction

The two extended foundations enable us to reduce the n trace inductance problem into 1-trace subproblems to solve the self L_p , and into 2-trace subproblems to solve the mutual L_p . There is *no* loss of accuracy during the reduction.

Therefore, we propose to build tables via numerical inductance extraction for self and mutual inductances.

There are two parts in the table-based inductance extraction. One is to pre-compute inductance tables. We assume that each layer has a nominal thickness, and build tables for different layers. The self inductance table has two dimensions: width and length. The mutual inductance table has three dimensions: widths for two traces and the spacing between them. The 3D inductance extraction tool RI3 [6,9] is invoked to solve a block of two traces with or without ground plane(s) in layer $N+2/N-2$ for different combinations of lengths, widths, and spacings. The resulting self and mutual inductance is stored in tables. Note that only 2-trace subproblems need to be solved, because results to 1-trace subproblems are parts of results to 2-trace subproblems. In addition, the inductance depends on the skin depth, which is a function of frequency [1]. We run RI3 under the significant frequency. The significant frequency is defined as $0.32/t_r$, where t_r is the minimum rising/falling time [1].

The other part of the table-based inductance extraction is table lookup. For each trace in a block, we obtain a self inductance from tables for a given layer, length and width. For any combination of two traces T_i and T_j ,

we obtain a mutual inductance from tables for a given layer, widths, and spacing between T_i and T_j . A bi-cubic spline algorithm [10] will be used to interpolate/extrapolate inductance that is not given in the table.

IV. Inductance Modeling for Cascaded Wire Segments

The discussion in the previous sessions were addressed to isolated multi-conductor systems with or without ground plane(s). The inductive couplings from other neighboring wires to the systems or vice versa are ignored. If there is no ground plane or ground mesh on chip, the inductive coupling (or return paths) may extend to very long range, the couplings may be significant. Hence, it is difficult to model the inductance for cascaded wire segments of a multi-conductor net. In this session, we will show from Raphael RI3 inductance extraction results that if a signal wire is guarded by two ground wires of *at least equal width* either on left and right in the same layer and with or without local ground plane(s), then this kind of multi-conductor systems may be linearly cascaded to determine the total effective loop inductance. In other words, the total loop inductance is the serial or parallel combination of the loop inductances of the cascaded segments determined individually. This conclusion indicates that those two guarded ground wires completely shield the inductive coupling between one multi-conductor system and its environment. This conclusion is important while applying the structure to high-speed clock design and will be discussed in the next session.

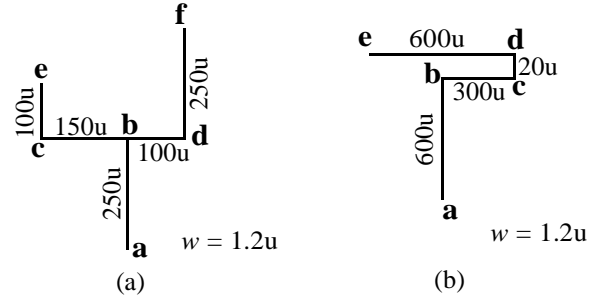


Figure 6: Two interconnect trees. Each segment of the trees is a three-same-width-wire multi-conductor system.

To show this linear cascadability, we performed Raphael RI3 extraction to determine the loop inductances of the two interconnects in Figure 6(a) and Figure 6(b). Each segment is composed of a three-wire multi-conductor system where a center signal wire sandwiched by two ground wires. Their widths w are

equal. The loop inductances thus determined are then compared with the results determined by serially or parallelly combining the loop inductance of each segment. For example, the loop inductance to be compared for Figure 3(a) is $L_{ab} + (L_{bc} + L_{ce}) \parallel (L_{bd} + L_{df})$, where each L is a loop inductance, determined independently from the others.

The comparisons are summarized in Table I. We would observe difference on the results if the inductive coupling going beyond each multi-conductor system, especially when significant portions of the systems are close-by. From the results in the table, we see the discrepancy is small (only about 3.5%), and hence, have the linearly cascading conclusion. In fact, we have run many examples with different spacings and lengths. No significant differences exist. Since the width of each ground wire is the same as that of the signal wire and the shielding will improve if wider ground wires are used, we have the *at least equal width* conclusion.

	Loop L from RI3	Eff. Loop L from S/P combination	Error %
Fig. 3(a)	0.140 nH	0.145 nH	3.57%
Fig. 3(b)	0.517 nH	0.525 nH	1.55%

TABLE I. Linear Cascading Comparisons.

V. Application of Efficient Inductance Modeling in Clocktree RLC Extraction

In some recent papers [3,11], the importance of extracting inductance along with RC for clocktree has been pointed out. Therefore in our application example, we will not focus on the importance of including inductance in the delay calculation but instead on the application of the efficient inductance modeling and relevant arguments for formulating RLC netlist for a clocktree. In general, without consideration of inductance in the clock skew calculation, the difference can be more than 10%. If there is ringing due to inductance effect on the clock signal, the result can be even devastating.

Figure 7 shows an example clock buffer H-tree schematic. We consider two kinds of interconnect configurations along the clocktree: co-planar waveguide design in Figure 8 and microstrip configuration in Figure 9. It's a common practice to have a local ground plane to shield further the inductive coupling from the adjacent layers [2]. We zoom into a segment, e.g. segment i , between adjacent levels of clock buffers of the H-tree in Figure 7 and extract RLC for the segment.

Basically we extract the resistance, capacitance, and inductance respectively for each segment in the sub-section as shown in Figure 7 given the geometry param-

eters via the pre-characterized capacitance and inductance table look-up as discussed in [4] and in previous sections respectively. Resistance is calculated analytically [4]. Depending on the clocktree shielding configurations as in Figure 8 or Figure 9 in individual segment, corresponding inductance values are obtained via interpolation from the inductance table. As experimentally proven in Section IV, we can formulate a RLC netlist for the whole passive portion of a clocktree between two levels of the clock buffers using cascaded segment method. However, we still have the following assumptions to complete the RLC netlist formulation for the whole clocktree.

First, the inductance (self or mutual) is not scalable with length as shown in [1]. Both self and mutual inductance are super-linear functions of the trace length. For example, if a segment length changes from 1000um to 2000um, the self- and mutual-inductances increase by about 2.2-2.4 times. Therefore, we tend to underestimate the inductance for a segment, for example, segment i in Figure 7. This is because that all the segments such as i , o , j , p , k , etc. are all connected so the inductance should be extracted from the whole length if there are no alternative return paths. However, from the argument in Section IV, we can neglect the mutual couplings between different segments such as between i and j , or i and k . Furthermore, there can be regular connections to the near by ground nodes (such as ground C4 bumps) from the shielding ground wire and therefore providing shorter return paths. Hence, our assumption on extracting inductance for each segment separately and then cascading them together along the path to formulate the RLC netlist is experimentally valid.

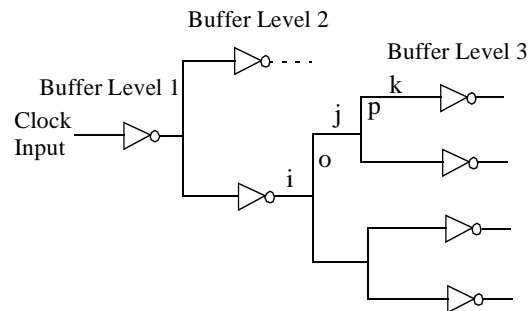


Figure 7: Example Clock Buffer H-tree Schematic

Second, how do we include the coupling effect from the other signal wires outside of a clocktree segment as shown in Figure 9? In our efficient inductance models, we can easily construct the RLC netlist for a N parallel wires as in Figure 8 or Figure 9. Therefore, the coupling

effect mainly inductive coupling of other signals next to the clocktree can be taken care of by simply adding them in the clocktree simulation.

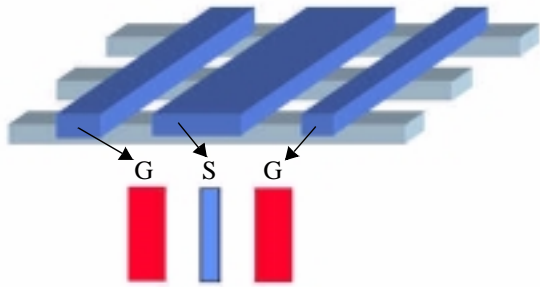


Figure 8: Co-planar waveguide configuration as a basic building block for clocktree signal distribution.

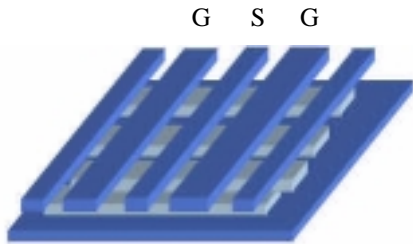


Figure 9: Microstrip configuration as another basic building block for clocktree signal distribution.

Since inductance is not sensitive to process variation as shown in [5], we can combine the nominal inductance with the statistically generated RC [4] in the formulation of RLC netlist in the study of process variation impact to clock skew.

VI. Discussions and Conclusions

In this paper, we have presented an extended table-based inductance extraction methodology as compared to the one in [5]. We also have applied it to a clocktree RLC netlist extraction with the observation of feasibility of cascaded RLC-segments in formulating the full RLC netlist for a clock tree.

However, our inductance models consider traces only in layer N, and layer N with ground planes in the neighboring layers. If there are parallel array of traces (may be signal traces or AC grounded traces) in the vertically neighboring layers as in layer N+2 or N-2, we currently ignore their inductive coupling to layer N traces assuming that they are statistically quiet.

Our inductance modeling ignores the return paths on the package. The low impedance metal on the package may reduce the inductance, making the result pessimistic. However, on the capacitance modeling, we assume each coupling capacitor to ground wire as a perfect grounded capacitor with one terminal connecting to the circuit ground node. This assumption is optimistic. Therefore, we think the over-estimate on the inductance can be compensated by this assumption and our result is still valid.

VII. Acknowledgments

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VIII. References

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